IN THE CLAIMS:

Please am nd claims 1, 3, 5, 6, 7 8 and 10, inclusive.

Please cancel claims 2, 4 and 9.

1. (Currently Amend d) A m thod for testing a multi-chip packag as a device und r t st in order to t st for intermittent or p rmanent short circuits and open circuits in th internal components comprising the steps of:

a10

(a) applying a rising temperature to the device under test while concurrently measuring the power bus to ground resistance during an up temperature ramp;

(b) ~~incrementally~~ reducing down the temperature of said device under test back to starting room temperature while monitoring and reading the power bus to ground resistance of the device;

(c) plotting a graph of the power bus to ground resistance of the device during the temperature up ramp and during the temperature down ramp~~.~~;

(d) noting the regularity or irregularity of the up ramp and down ramp temperature graphs plotted against the power bus to ground resistance in order to determine the operability or defectiveness of components within the multi-chip package.

2. (Cancelled).

A 10 Cont'd

3. (Currently Amended) A method for testing internal components of an integrated circuit package having an internal power bus, said method comprising the steps of:

Q3 Cont'd

(a) cycling the ambient temperature around said integrated circuit package from room temperature up to a higher selected temperature and then back again to room temperature;

(b) reading out the power bus-ground resistance at selected intervals during the up-ramp temperature change and during the down-ramp temperature change;

(c) plotting a graph of the power bus-ground resistance against temperature during the up-ramp and down-ramp temperature change~~.~~;

(e) observing an erratic characteristic of the plotted graph to indicate a defective component that is intermittently shorted or open-circuited.

4. (Cancelled).

A3 Cont'd

5. (Currently Amended) The m thod of claim 3 wherein step B(b) includ s the step of:

(b1) controlling a Peltier-junction modul to act as an increasing heat source or as a ~~decreasing~~ heat sink to decrease the operating temperature.

A3 Cont'd

6. (Currently Amended) A method for t sting the int grity of int rnal components of an integrat d circuit packag constituting a device und r test and having an internal power bus, comprising the steps of:

93 Cont'd

(a) setting a metallic transfer block unit at a normal room temperature;

(b) attaching a device under test to said transfer block and connecting internal ~~said~~ power bus-to ground connections ~~internal connections~~ of said device under test to a digital multimeter;

(c) utilizing a computer program for sequencing the temperature of said device under test into an upward temperature rise and subsequently into a downward temperature drop back to room temperature, while concurrently reading the power bus-to ground resistance every 2 seconds during the up-ramp cycle and the down-ramp cycle;

(d) plotting, on a computer screen, the said resistance readings during the up-ramp temperature cycle and the down-ramp temperature cycle;

(e) reading the plotted graph on said computer screen of the power bus-to ground resistance against the temperature up-ramp and down-ramp cycles in order to differentiate a normal set of workable components in said integrated circuit package from intermittently defective ~~in order to differentiate inoperable~~ open-circuited or short-circuited components within said integrated circuit package. ~~module.~~

7. (Currently Amend d) An apparatus for t sting internal components of an integrated circuit packag , having an internal power bus, to det rmine normal op ration or problem areas in said components, comprising:

A3 Cont'd

(a) means for temperature cycling said package over a normally non-destructive range of room temperature to 20 degrees Celsius upward and 20 degrees Celsius downward to room temperature without opening up said package;

(b) computer means for logging a graph of said power bus to ground resistance against the temperature during the temperature cycle~~,~~ said logging occurring every two seconds during said temperature cycle;

(c) means for analyzing said graph to determine normal operation or problem areas in said package.

8. (Original) The apparatus of claim 7 wh r in said means for temperature cycling includes:

(a1) a computer g n rat d s quencing program to control a P ltier thermoelectric module to act as a heat source and/or heat sink to said package under test.

A3 Cont'd

9. (Canc lled).

A3 Contd

10. (Currently Amend d) An apparatus for t sting internal components of an int grated circuit package devic under t st to determine normal op ration or problem areas in the components, said apparatus comprising:

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(a) test socket means for connecting the device under test with a digital multimeter in order to measure the power bus-to ground resistance of the internal components;

(b) temperature transfer block means connected to a temperature meter for placement adjacent said device under test in order to increase the ambient heat or decrease the ambient heat to said device under test;

(c) a Peltier-thermal electric module adjunct said transfer block means and connected to a programmable power supply for controlling the addition of heat to, or reduction of heat from, said temperature transfer block;

(d) heat sink and fan means placed adjunct to said Peltier thermal electric module and connected to a programmable controlled fan power supply;

(e) computer means having a control program for connection and management of said programmable controlled fan power supply, said programmable power supply ~~and~~ for sensing operations of said temperature meter and said digital multimeter to controllably enable ~~the~~ said computer means for sequencing of an up-ramp temperature and a down ramp temperature adjacent said device under test, while concurrently reading-out and plotting the power bus-to ground voltage during the

A3 cont'd

up-cycle and down-cycle of th temperature applied to said device under t st.